

SG320200A (320 DOTS X 200 DOTS)

FEATURES

- ◆ NO BUILT-IN CONTROLLER
- ◆ 4.5V POWER SUPPLY
- ◆ +3.3V POWER SUPPLY
- ◆ 1/200 DUTY CYCLE
- ◆ 4-BIT PARALLEL INTERFACE

INTERFACE PIN CONNECTIONS

NO.	SYMBOL	LEVEL	FUNCTION
1	EL1	-	EL Backlight
2	EL2	-	EL Backlight
3	NC	-	No Connection .
4	V _{DD}	3.3V	Power Supply Voltage
5	FLM	H	Frame Start Signal
6	M	H/L	Control Signal For AC Driving
7	CL1	H→L	Common Driver Data Shift Signal
8	/DISPOFF	H/L	Display OFF.Active LOW
9	V _{SS}	0V	Power Supply Ground
10	CL2	H→L	Clock Pulse For Segment Shift Register
11~14	DB3~DB0	H/L	Data Bus Line
15	V _{DD}	3.3V	Power Supply Voltage
16	V _{SS}	0V	Power Supply Ground

MECHANICAL DATA

ITEM	DIMENSIONS	UNIT
Module Size (W x H x T)	110.4 x 57.0 x 7.4	mm
Viewing Area (W x H)	82.0 x 46.0	mm
Active Area (W x H)	80.0 x 44.0	mm
Dot Size (W x H)	0.22 x 0.195	mm
Dot Pitch (W x H)	0.25 x 0.22	mm

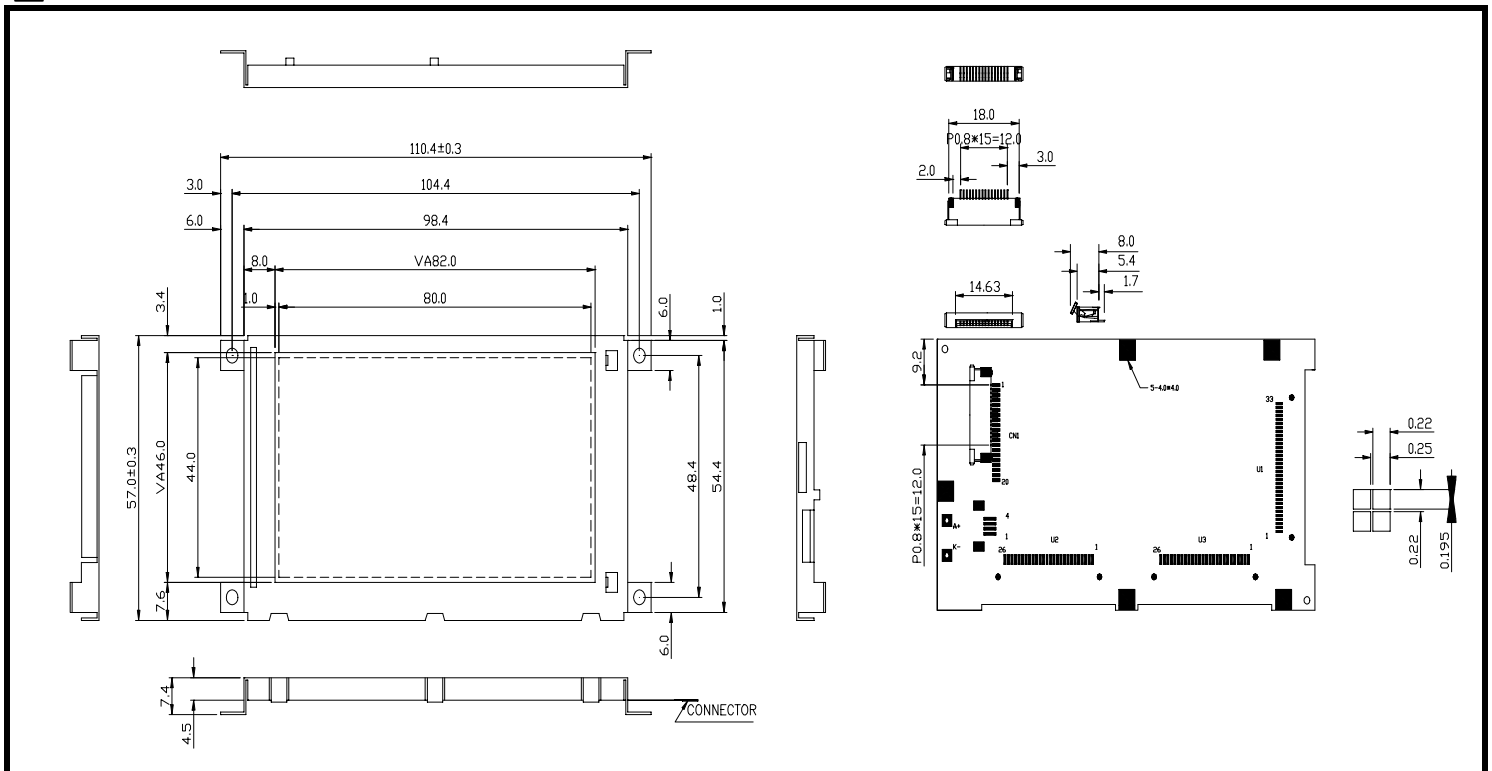
ABSOLUTE MAXIMUM RATINGS

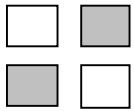
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	V _{DD} -V _{SS}	0	-	7	V
Supply Voltage For LCD Drive	V _{DD} -V _o	0	-	30	V
Input Voltage	V _I	V _{SS}	-	V _{DD}	V

ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage For Logic	V _{DD} -V _{SS}	-	2.7	3.3	4.5	V	
LCD Supply Voltage	V _{DD} -V _o	V _{DD} =3.3V Ta=25°C	19.8	22.1	23.4	V	
Supply Current	I _{DD}	V _{DD} =3.3V	-	4.5	6.5	mA	
Input	"HIGH" Level	V _{IH}	-	2.2	-	V _{DD}	V
Voltage	"LOW" Level	V _{IL}	-	-	-	0.6	V
Output	"HIGH" Level	V _{OH}	-	2.4	-	-	V
Voltage	"LOW" Level	V _{OL}	-	-	-	0.4	V

EXTERNAL DIMENSIONS

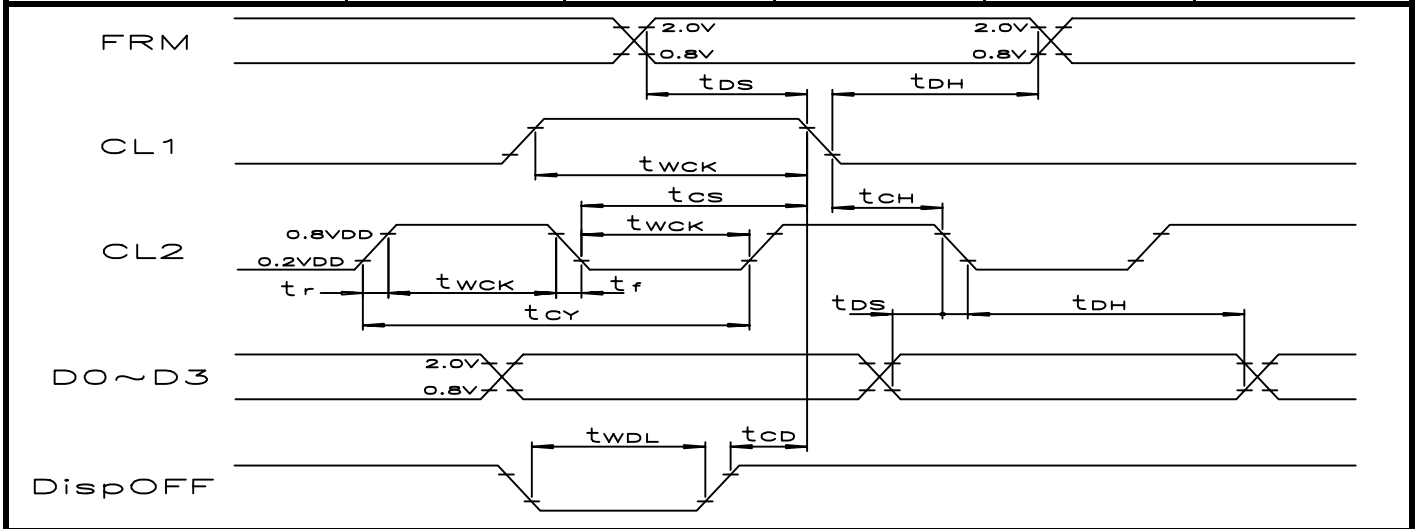




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TIMING CHARACTERISTICS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
Clock cycle time	t_{CY}	Duty=50%	250	-	ns
Clock Pulse Width	t_{WCK}		95	-	ns
Data Set Up Time	t_{DS}		65	-	ns
Data Hold Time	t_{DH}		65	-	ns
Latch pulse 'H' width	t_{WCK}		95	-	ns
Input signal Rise/Fall Time	t_r, t_f		-	30	ns
Clock Set Up Time	t_{CS}		120	-	ns
Clock hold time	t_{CH}		120	-	ns
FRM set-up time	t_{DS}		30	-	ns
FRM hold time	t_{DH}		30	-	ns
DispOFF clear time	t_{CD}		100	-	ns
DispOFF 'L' pulse width	t_{WDL}		1.2	-	μs



BLOCK DIAGRAM

